APPENDIX A

In the following pages, pictures of various hardware modules of the system are presented. The illustrations are in the following order:

Pulsar Search Preprocessor:

- Input Selector for Search Pre-processor (ISSP)
- Search Pre-processor (SP) module
- Data collection card for pulsar search pre-processor (PSP)
- The PSP after assembly

Portable Pular Receiver:

- Sampler and Bit-packing module for Portable Pulsar Receiver

Signal Processor for Pulsar Studies:

ADC module for two polarization channels

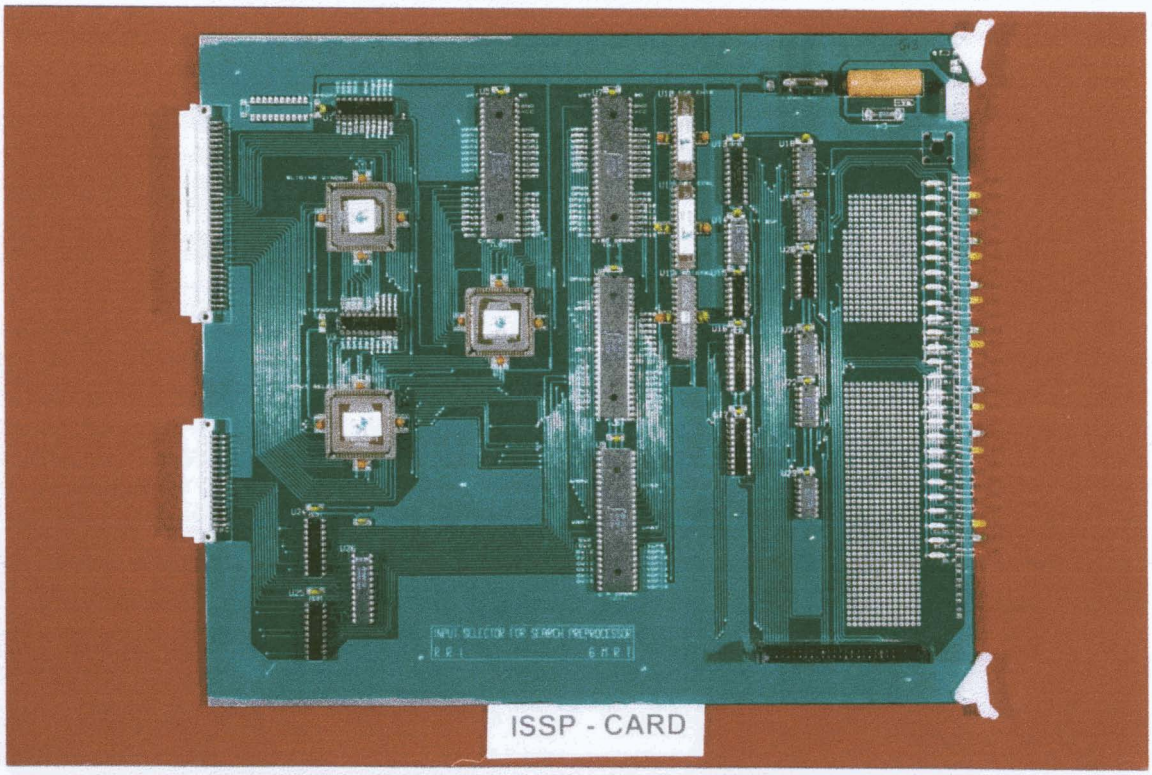
- Plessey FFT module for two polarization channels
- Sampler and FFT module (after assembly) for SPPS
- Polarimeter module for SPPS
- 4-node DSP module for SPPS

8K x 48 bit OPRAM module for DSP nodes.

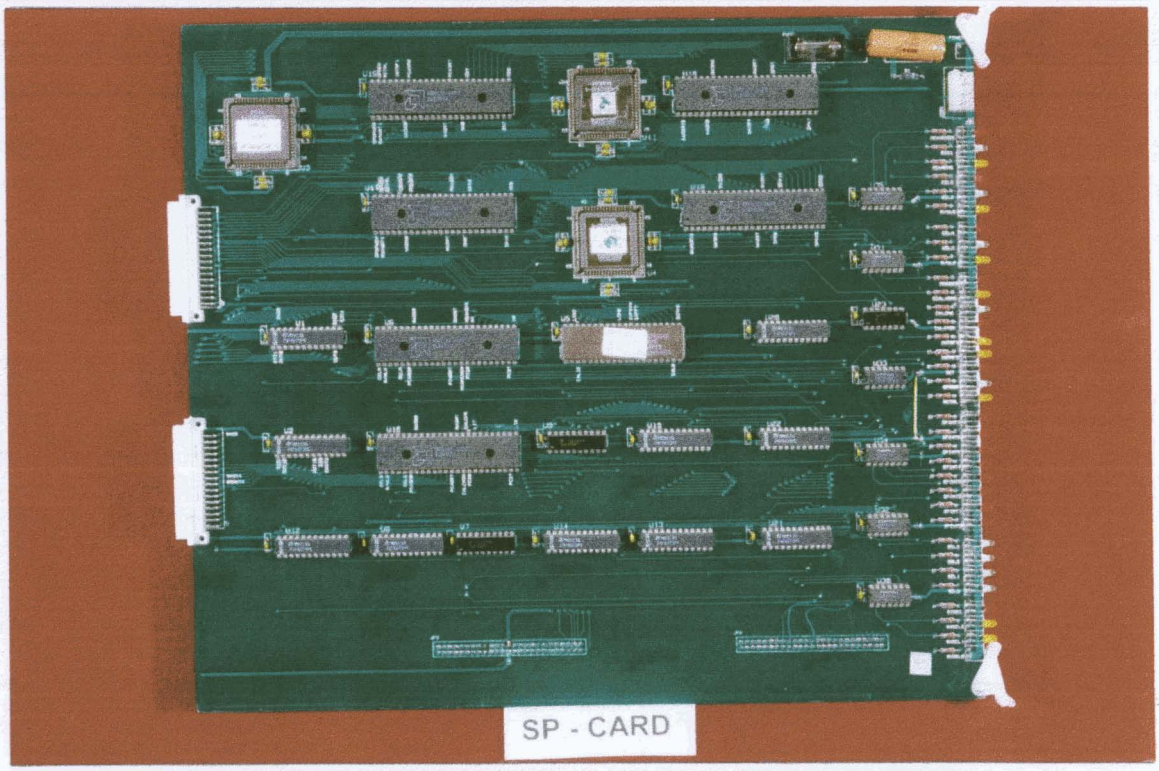
32 bit FIFO module for DSP nodes.

Data Acquisition module for SPPS.

The SPPS after assembly.

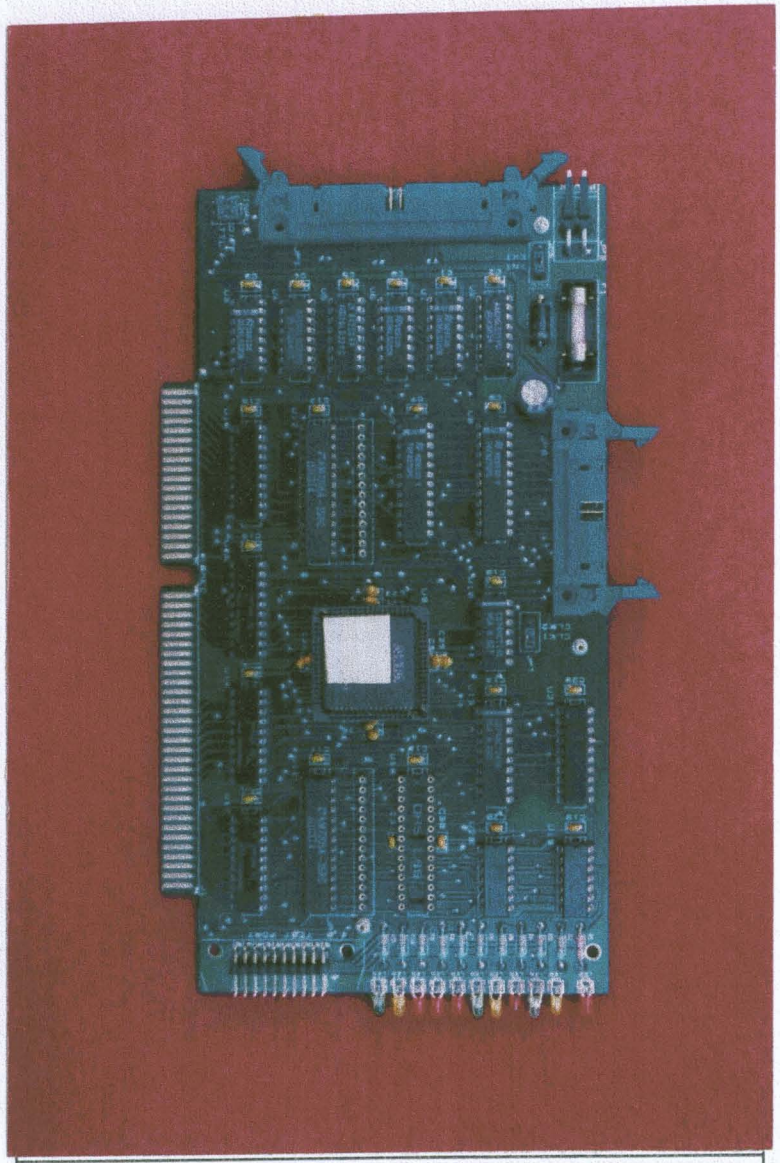


Input Selector for Search Pre-processor (ISSP)



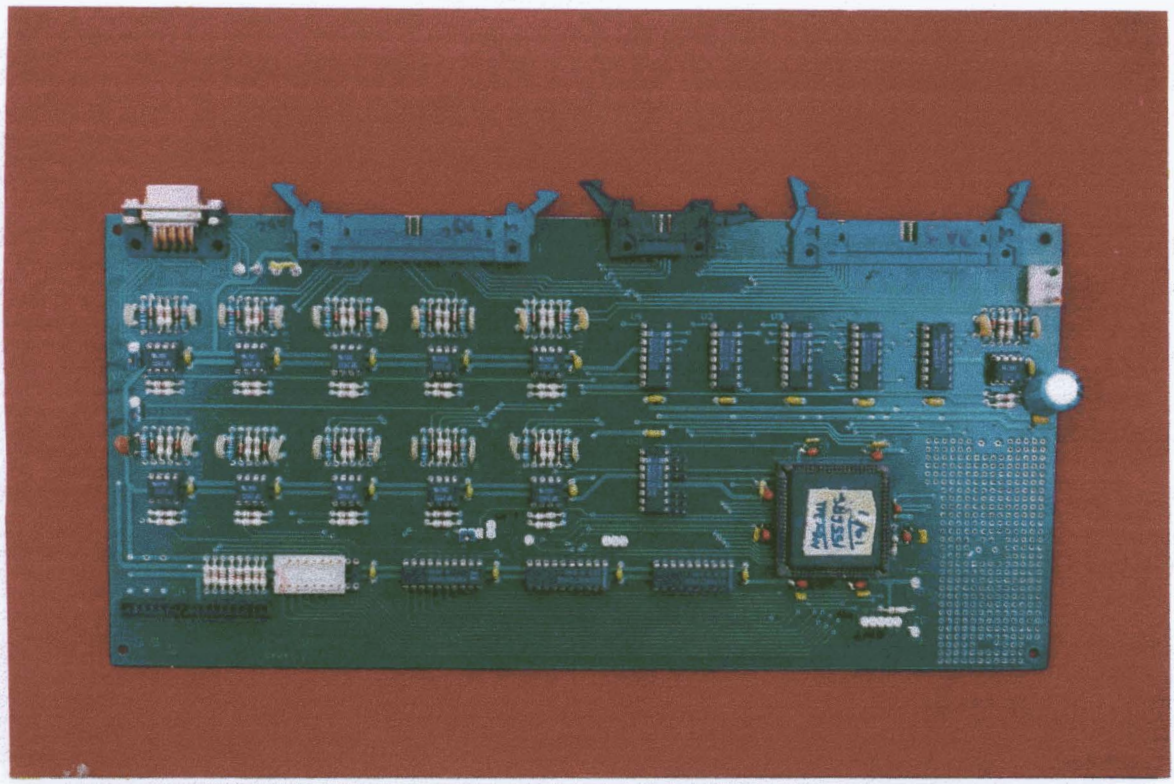
Search Preprocessor (SP) module

The PSP after assembly

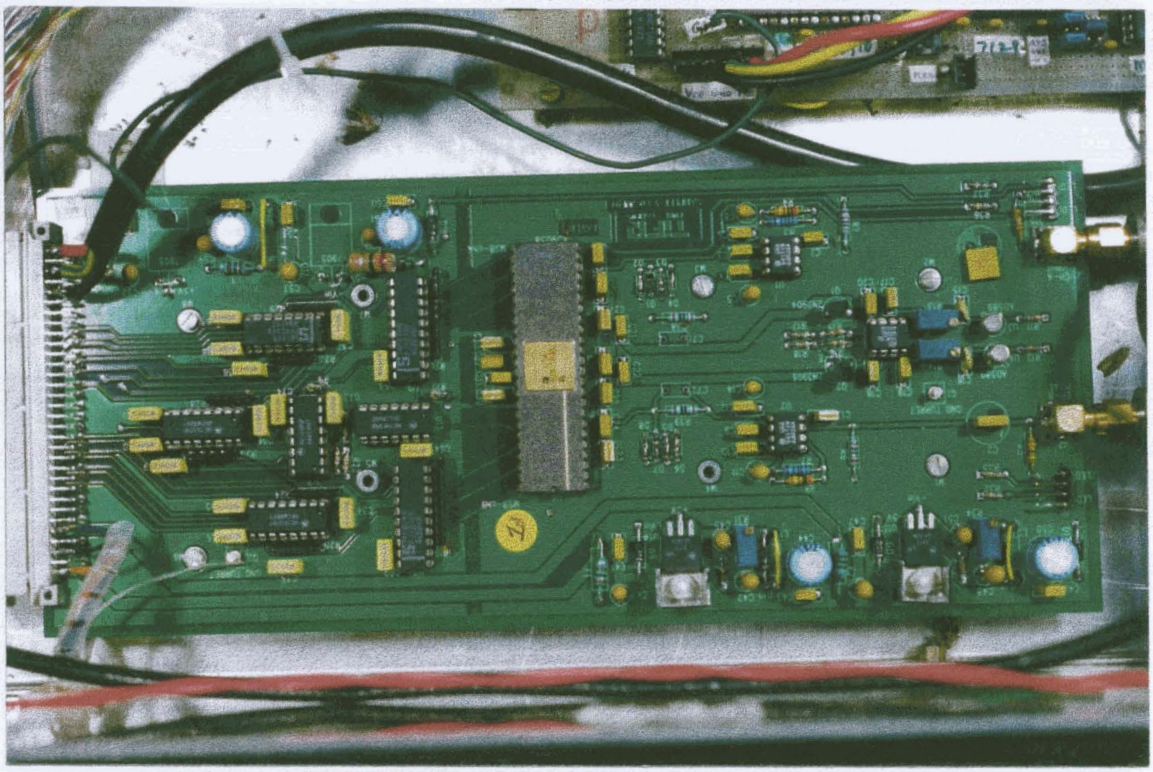


Data collection card for pulsar search pre-processor (PSP)

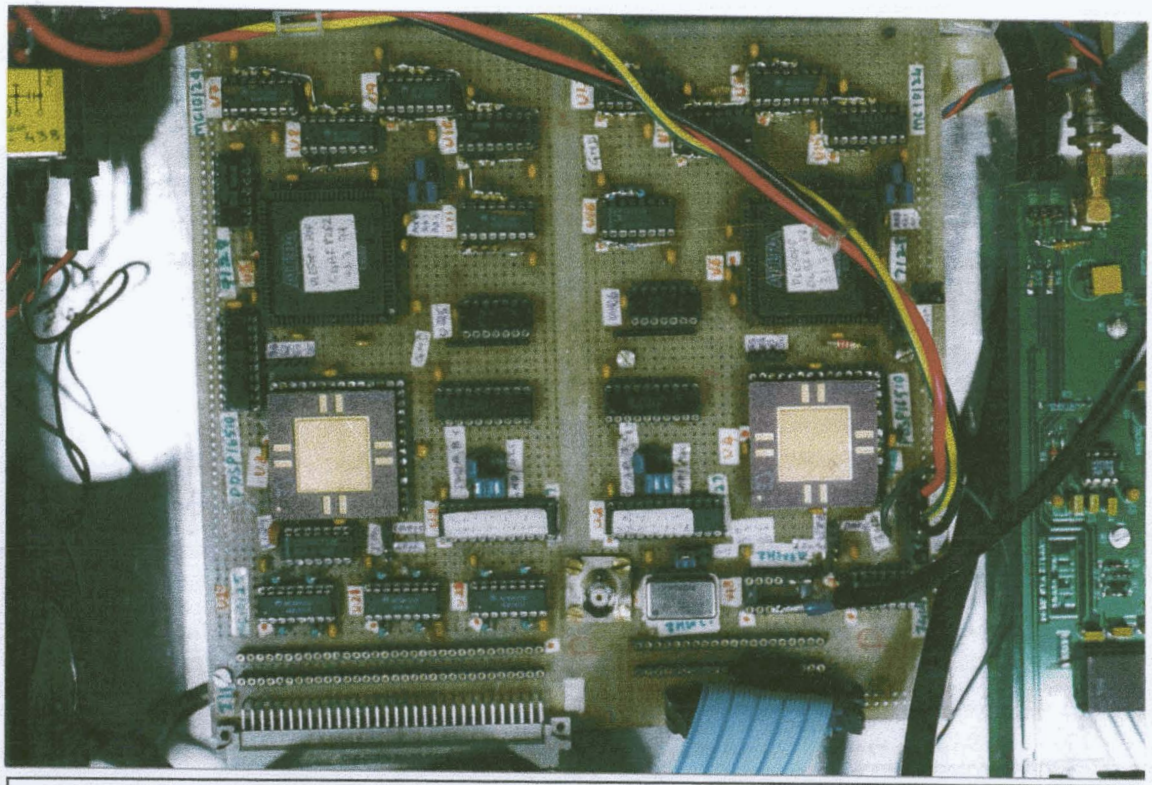
The Signal Processor for Pulsar Studies (SPPS) reduces the distortions caused by the effects of Dispersion, Faraday rotation, Doppler acceleration and parallactic angle, at a sustained data rate of 32 Msamples/sec. It also folds the pulses coherently over the period and integrates adjacent samples in time and frequency to enhance the signal to noise ration. The resulting data is recorded for further off-line analysis of the characteristics of pulsars and the intervening medium. The signal processing for analysis of pulsar signals is quite complex, imposing the need for a high computational throughput, typically of the order of a Giga Operations Per Second (GOPS). Conventionally, the high computational demand restricts the flexibility to handle only a few type of pulsar observations. This instrument is designed to handle a wide variety of Pulsar observations in association with the Gaint Metre Wave Radio Telescope (GMRT), and is flexible enough to be used in many other high-speed, signal processing applications. The technology used includes field-programmable-gate-array (FPGA) based data/code routing interfaces, PC-AT based control, diagnostics and data acquisition, Digital Signal Processor (DSP) chip based prallel processing nodes and C language based control software and DSP-assembly programs for signal processing. The architecture and the software implementation of the parallel processor are fine-tuned to realize about 60 MOPS per DSP node and a multiple-instruction-multiple-data (MIMD) capability.



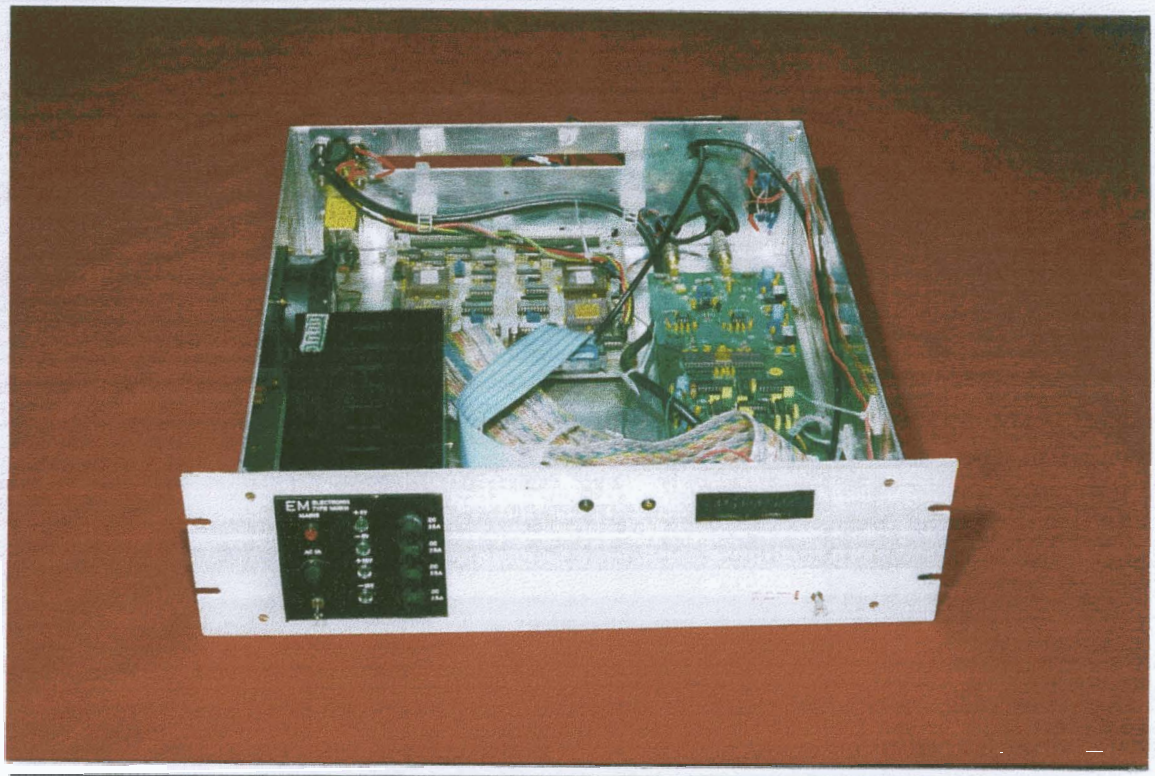
Sampler and Bit-packing module for Portable Pulsar Receiver



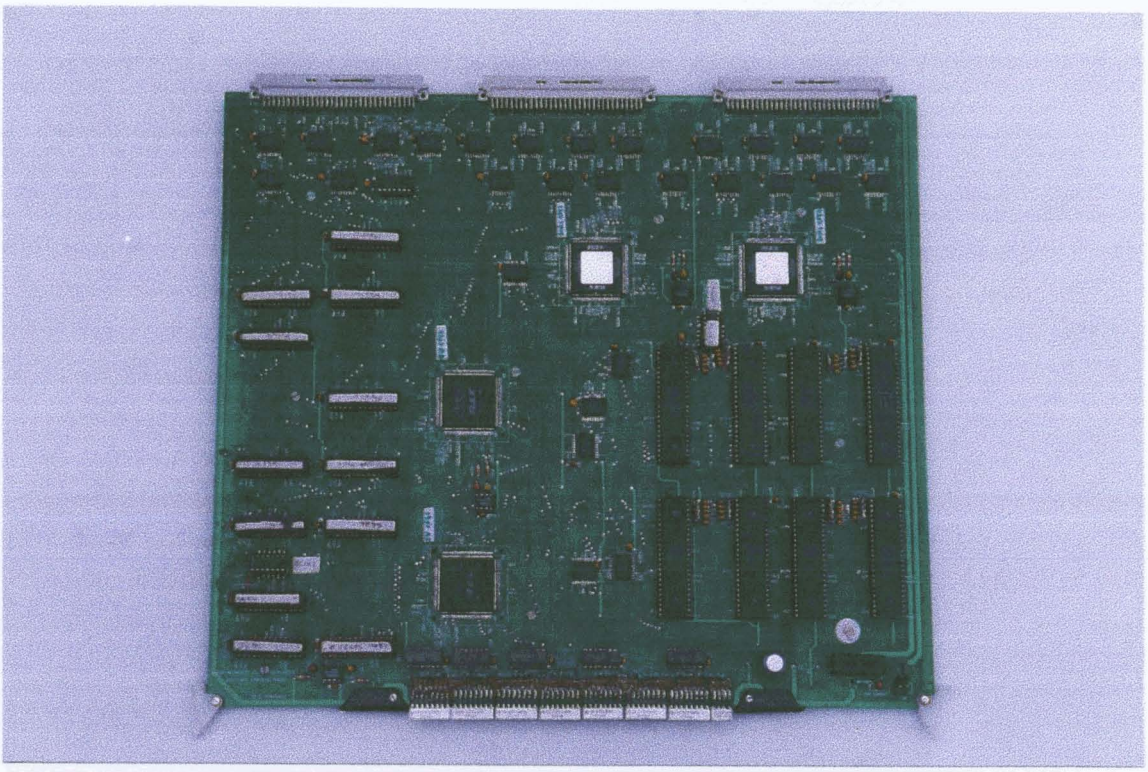
ADC module for two polarization channels



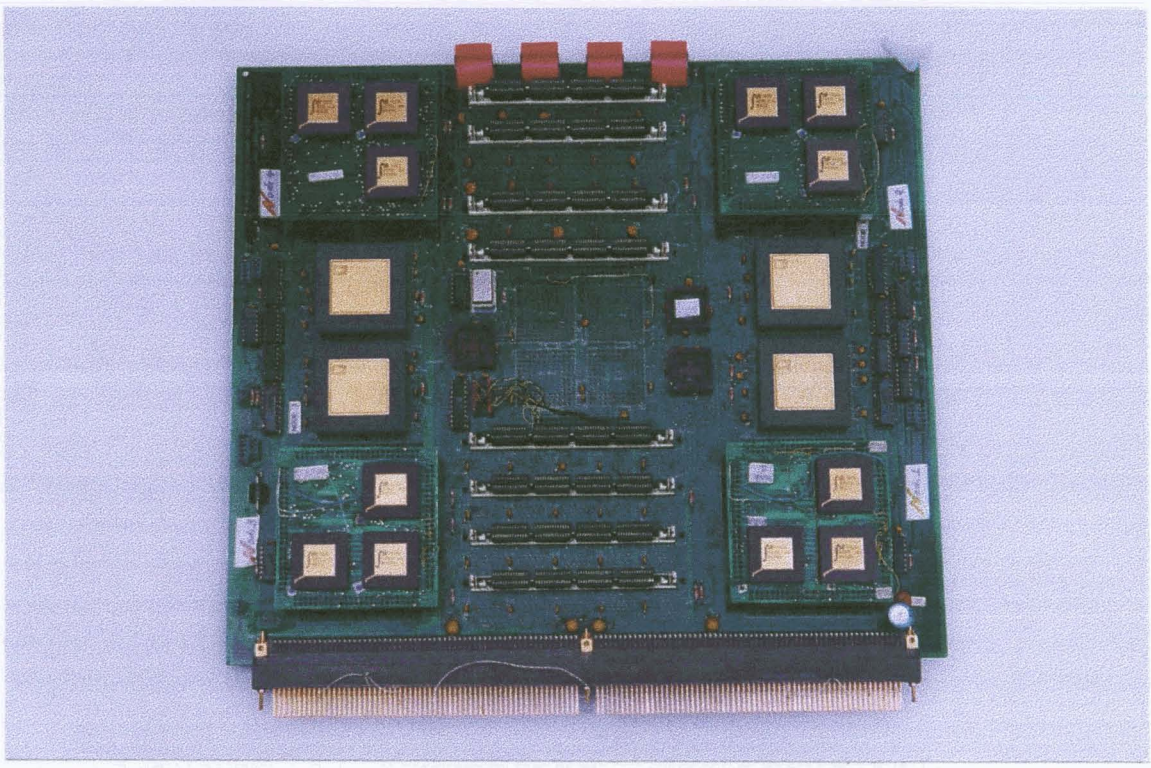
Plessey FFT module for two polarization channels



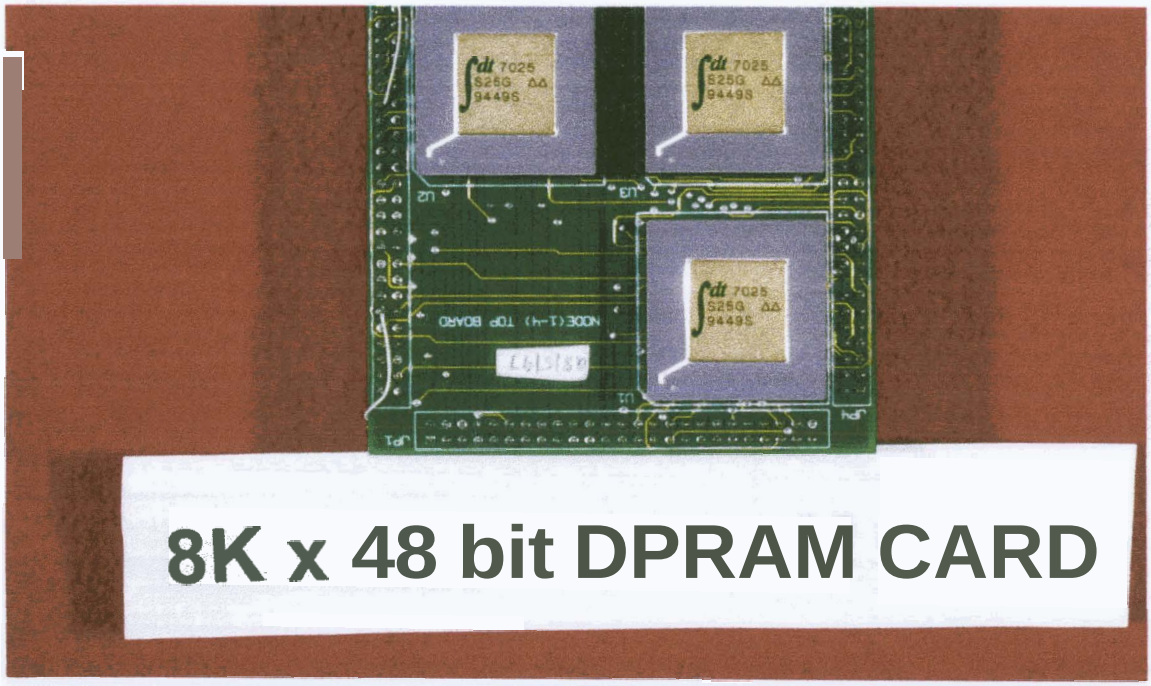
Sampler and FFT module (after assembly) for SPPS



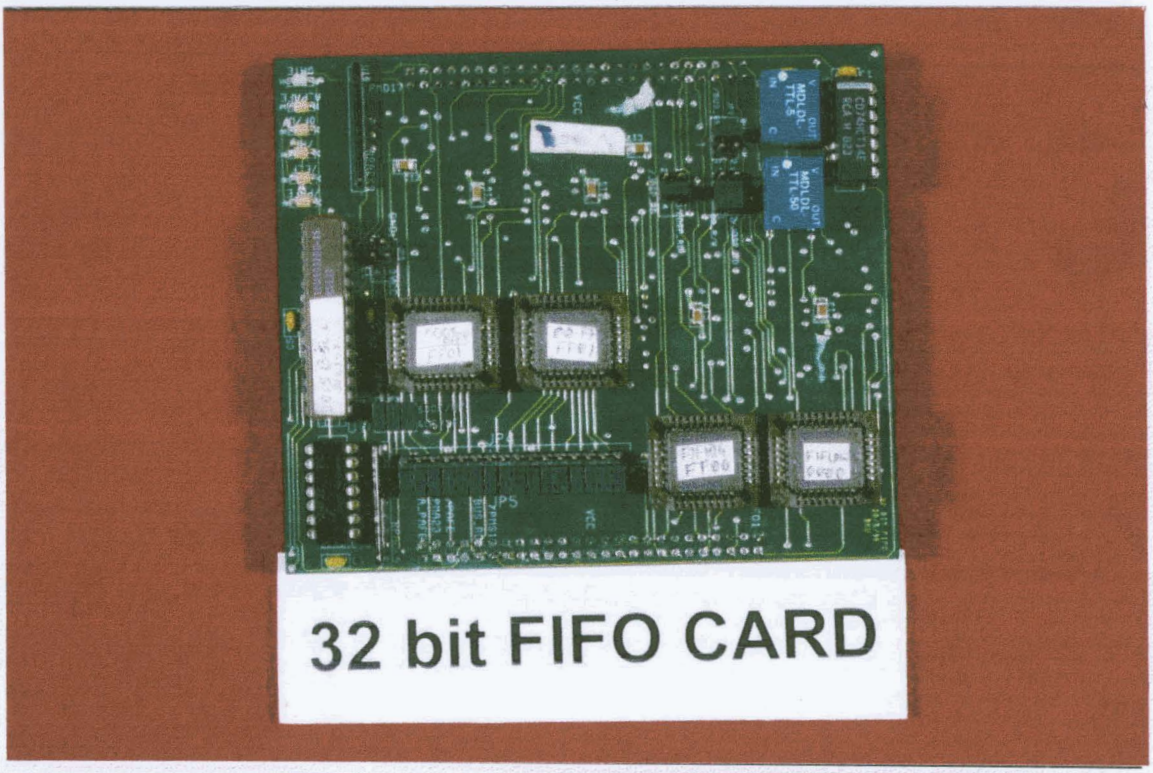
Polarimeter module for SPPS



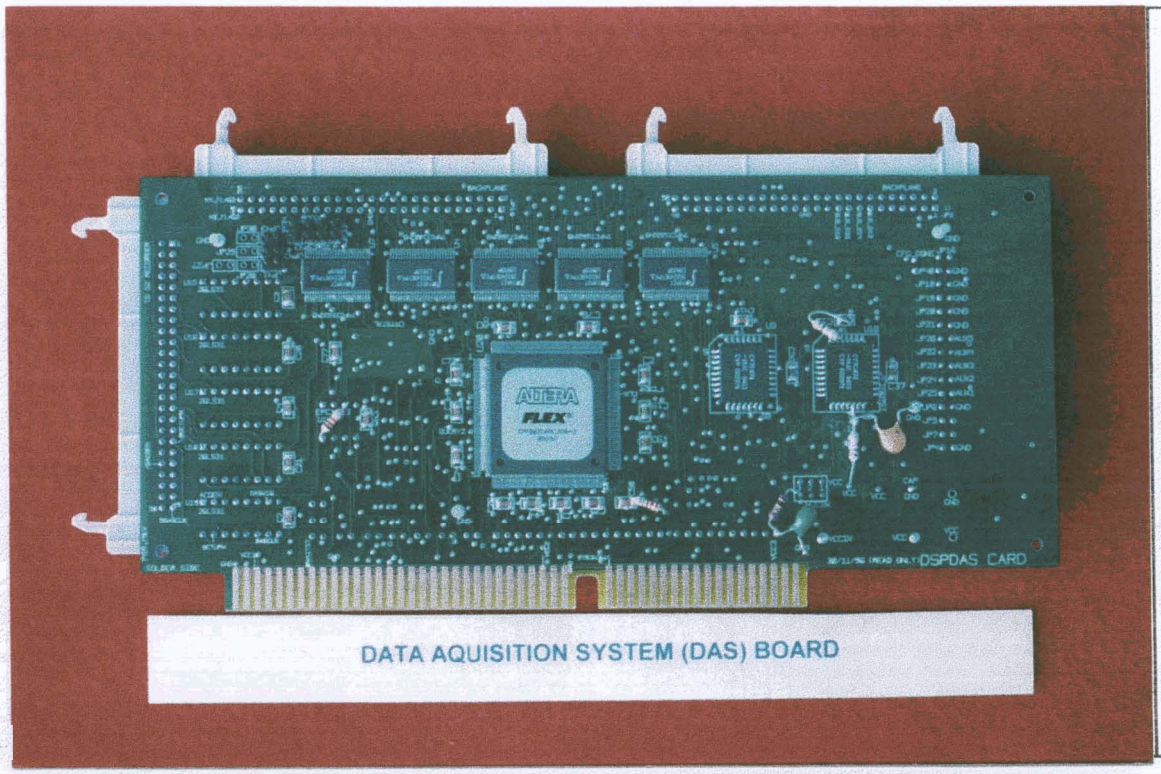
4-node DSP module for SPPS.



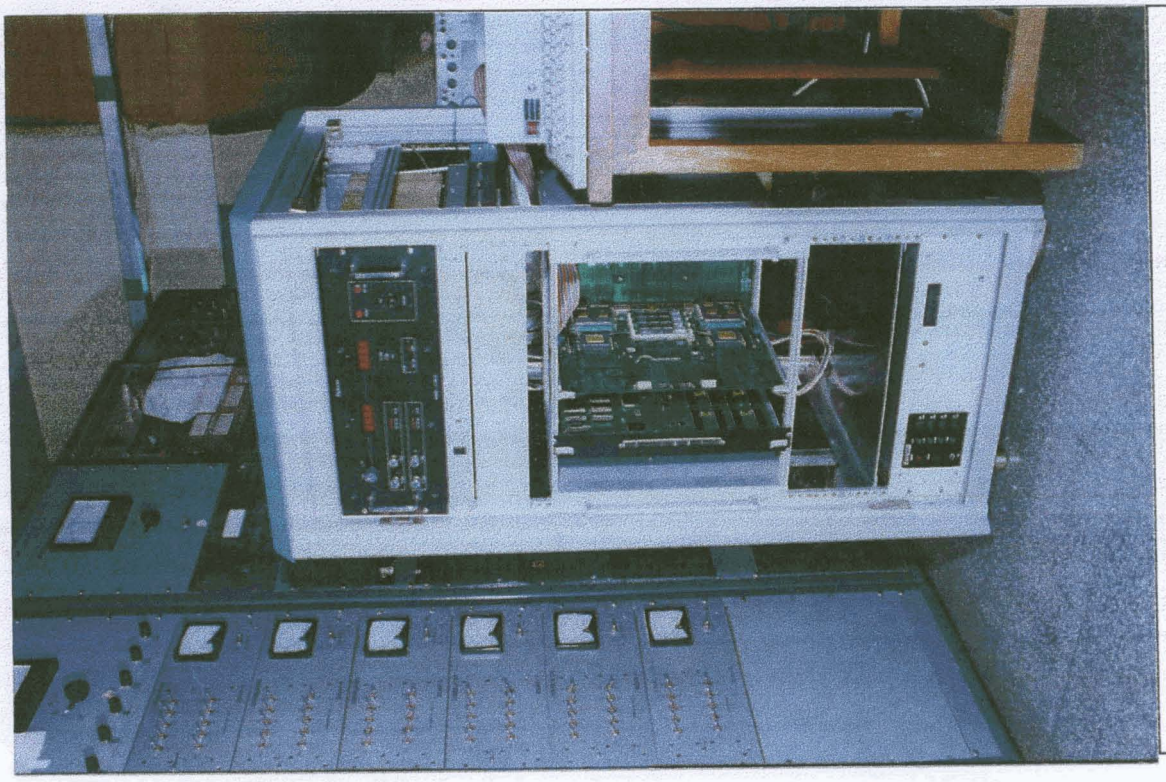
8K x 48 bit DPRAM module for DSP nodes.



32 bit FIFO module for DSP nodes.



Data Acquisition module for SPPS.



The SPPS after assembly.