CHAPTER – III

ANALYSIS AND DESIGN

3.1 Specifications

As is evident from the discussions in the previous Chapter, instruments based on *PCs* have many advantages over their conventional counterparts. Hence, PC based data acquisition, storage and analysis was chosen for the on-going radio *interferometer* project as *already* explained. Apart from providing a test bench for trying out *several* new techniques, both in the field of RF signal processing and PC based data acquisition, this radio in*terfer*ometer is expected to provide useful data *regarding* the phase stability of the entire system over several days. It is foreseen that by fitting the fringes obtained for the same radio source over several days, the ionospheric disturbances at the operating frequency could also be studied. Table 3.1 gives the overall characteristics of this radio interferometer. While conventional techniques are followed in developing the interferometer, the use of a PC in the instrumen*tation* for this system is a departure from present day interferometers. Hence the RF, IF and receiver sections were chosen to be realised using readily available components wherever possible; but a dedicated **DAS** was designed to suit the signals for optimum performance of the *overall* system. The detailed specifications of the various building blocks of this system with special emphasis on the **DAS** axe now discussed. The experimental work pertaining to the various building blocks of the entire radio interferometer is discussed in Chapter N.

3.1.1 Field and Receiver System : As seen from Table 3.1, the RF section of

TABLE 3.1

RADIO INTERFEROMETER - OVERALL CHARACTERISTICS

Parameter	Specifications	Remarks
Operating frequency	80 - 160 MHz, tunable	To complement astronomical data in other bands
Tunability	± 5 MHz over a chosen frequency	To tune out interference, if any
Baseline	700 m E - W	Transit instrument
Collecting area	$16X^2 + 16\lambda^2$ (32 elements)	Minimum for required sensitivity
Sensitivity	250 x 10^{-26} $watts/m^2/Hz$	Appendix A

the interferometer requires two chains of two distinct blocks, viz., antennas and associated RF units in the field and receiver units at the central laboratory. Figs. 3.1 and *3.2* give the detailed block schematics of this system. As shown, the first Superheterodyning is carried out in the field. This enables easy transmission of the received *signal from* the field to the central laboratory at first IF, while ensuring good image rejection. This is followed by the second Superheterodyning in the Laboratory, which facilitates good tunability for interference rejection and ease of operation at lower *frequencies.* The technical specifications are now summarised in Table **3.2.**

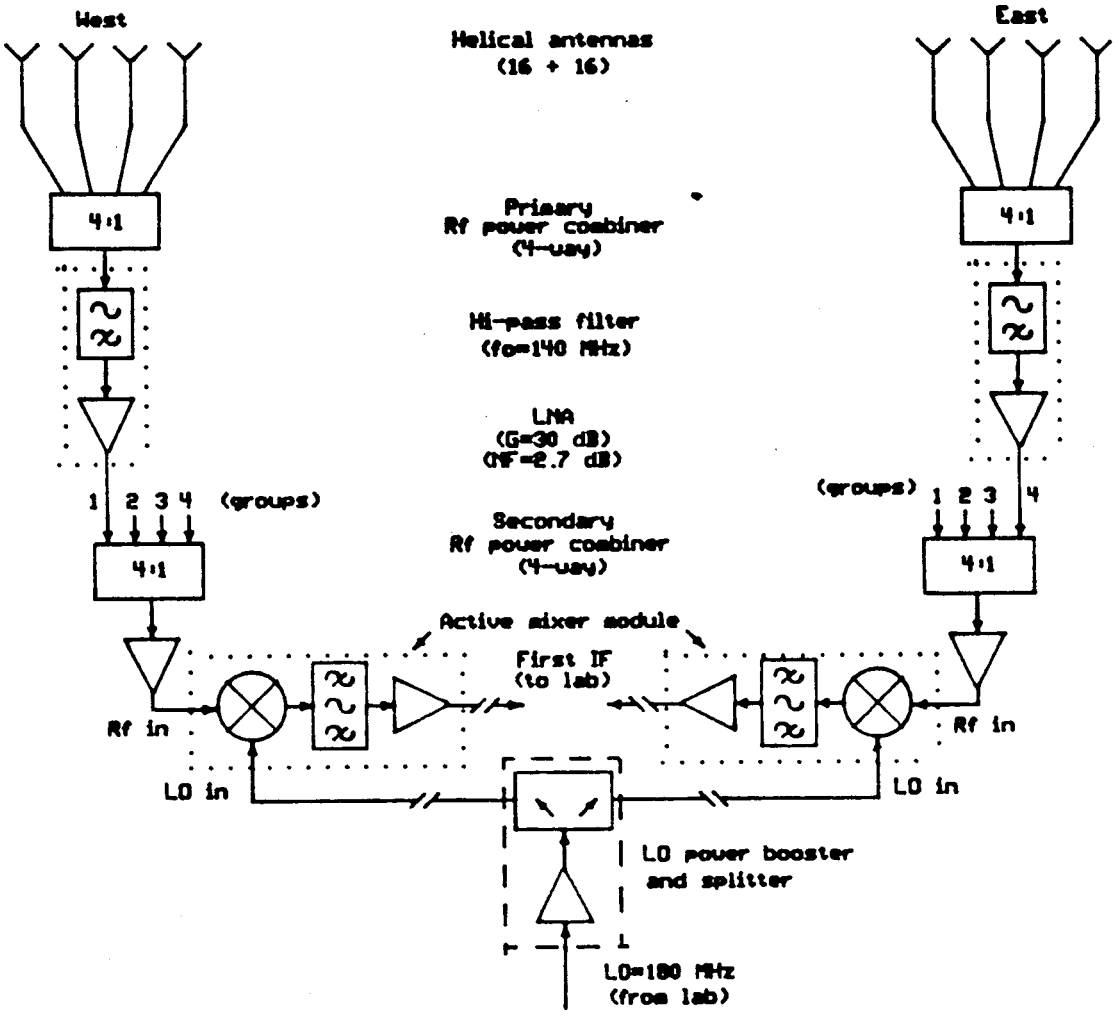
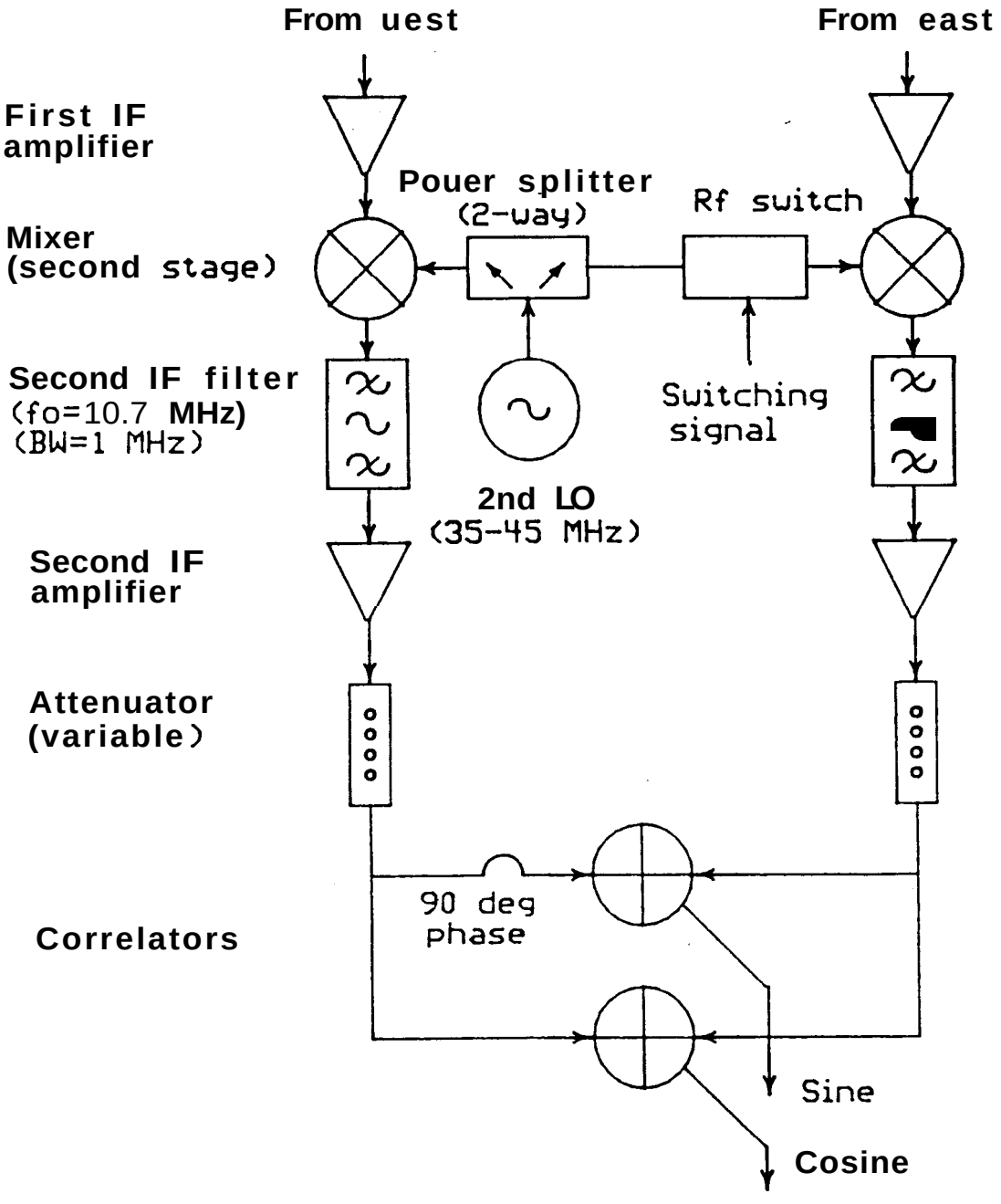


Figure 3.1 Radio Interferometer - Receiver System: Field Unit



Fiqure *3.2* **Radio Interferometer – Receiver system: Lab Unit**

TABLE 3.2

RADIO INTERFEROMETER - TECHNICAL SPECIFICATIONS

Building Blocks	Characteristics	Remarks
Antenna	Broad band; atleast one octave	Helical antenna suitable
R F pre-amplifier	Gain = 30 dB NF = 260^0 K BW = DC - 250 MHz	Sky temperature at 150 MHz $\approx 250^0$ K
Double super-heterodyne receiver First LO First IF Second LO Second IF	frequencies(MHz) 185, for RF at 150 35 45.7 $\pm$ 5 (tunable) 10.7	In the field; Two stage for good image rejection; In the lab; To facilitate interference rejection
Correlator	2 channel;configurable as adding or multiplying type	Analog system; Better S/N than digital system

The outputs of these two chains at the 2nd IF finally lead to a two-channel analog correlator. The correlator multiplies the signals from the two chains, both in amplitude and in phase to produce fringes as the earth rotates. This signal goes through a phase sensitive detector (PSD), to yield an output which is corrected for the periodic phase reversal introduced in the second local oscillator in one of the chains. This phase switching helps in the removal of gain instabilities in the RF/IF sections of the interferometer.

Typical specifications of this signal are given in Table 3.3. This signal serves as the input for the PC based *DAS*, so as to provide various features in the operation of the radio interferometer as envisaged earlier.

TABLE 3.3

CORRELATOR OUTPUT - SPECIFICATIONS

Parameter	Magnitude	Remarks
Ouput voltage range	1 mV - 1 V	From noise to fringe peak
Receiver noise	1 mV	Without terrestrial interferance
Fringe period	40 sec	At transit
No. of Fringes	43	For source transiting in zenith
PSD time constant	1 s	For all sources

3.1.2 DAS : The analog data output of the *PSDs*, corresponding to the Sine and Cosine channel correlators is a time varying signal corresponding to the fringes. This signal has to be sampled, quantized and accumulated for further processing and study. The DAS has an important role to play in acheiving this. Here, the main function of the DAS is to multiplex the analog signals in the two channels on a time division basis, sample them at

a required rate, to follow with suitable amplification and A/D conversion. The digital code, which is now a measure of the input signal is required to be stored in a suitable memory device. The block schematic of this DAS is shown in Fig. **3.3** and its specifications including the memory requirements are presented in Table 3.4.

TABLE 3.4

DAS - SPECIFICATIONS

Parameter	Value	Remarks
Number of inputs	**2**	**Sine and Cosine correlator**
Sampling period	**100 ms**	**Derived from siderial clock**
Gain range	**1 - 50**	**Programmability preferred**
Quantization levels	**1023 (10 bit)**	**To suit dynamic range of 30 dB**
Data storage requirement	< 40 Kbytes	For single radio source

3.1.3 Data Analysis Computer : The data acquired by the DAS, which is now available in a suitable storage device has to be *analysed as* described earlier. Some of the features of the computer required for *this* function are summarised in Table 3.5.

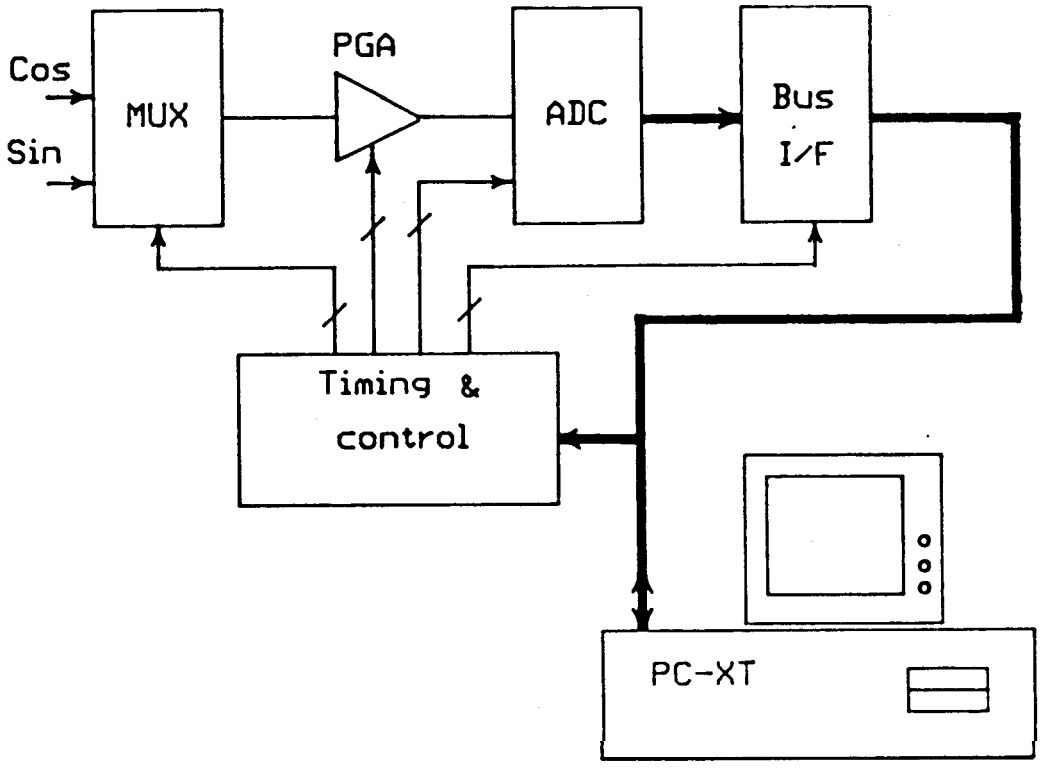


Figure 3.3 **Data Acquisition system** - Block **Schematic**

TABLE 3.5

DATA ANALYSIS COMPUTER - REQUIREMENTS

Function	Requirements	Remarks
Data storage capacity	30 Mbytes	For 30 days for 25 radio sources at 40 Kbytes for each source
Display facility	Graphics capability	Possibile with EGA on PC-XT
Ionosphere study	High CPU speed; String manipulation capability	For comparing data through large disk memory

3.2 Analysis

Major building blocks that constitute the DAS are shown in Fig. **3.3.** Considering the availability of both linear and digital *ICs* of a wide variety which are suitable to realise these building blocks, it is most appropriate that standard *ICs* are chosen for use here. As the system has to handle different types of signals at different stages, viz. low level analog voltages at its input, TTL level signals at its output etc., the *ICs* chosen can belong to different families. This *calls* for proper interfacing between them while *organising* the total system. While most of these functions can be realised using hardware, some units, especially timing and control, are preferably realised through software using the host PC. This approach not *only* reduces the *hardware* requirements, but *also* incorporates *flexi*bility and improved reliability in

the system operation. This is now briefly discussed and analysed block by block.

3.2.1 Multiplexer : As the signal level to be handled by the MUX is very low, care has to be exercised in the proper choice of the multiplexer. For efficient signal transfer, the ON resistance of the MUX should be as low as possible. As seen from Table 2.8, a relay based MUX provides almost zero ON resistance; but a CMOS IC MUX is more suitable here for the following reasons:

a) Availability in IC form

b) TTL compatible input select control

c) Built-in input protection

d) Low switching time

e) High inter channel isolation, hence low cross talk

f) CMOS technology, leading to better noise immunity

Some of the important electrical characteristics of the MUX type IH5116 (Intersil USA) suitable for this application are summarised in Table 3.6. The pinout details are provided in Appendix B. Though the requirement is to multiplex only two channels, a 16 channel configuration is preferred here to cater to future expansion possibilities and also to make the input stage of the DAS more general purpose.

3.2.2 S/H Circuit : As already indicated earlier, the S/H circuit looks at the analog signal at periodic time intervals and retains the amplitude information for a certain time duration to enable the ADC to process the signal further. Sampling is possible here using the MUX itself. A separate hold circuit is considered unnecessary in this application for the following reasons. For

TABLE 3.6

MUX - ELECTRICAL CHARACTERISTICS

Parameter	Value (typical)	Remarks
ON resistance	500 Ω	Low values preferred
OFF resistance	10^{10} Ω	High values preferred
ΔR_{on}	25 Ω	Lower the better
Switching time	< 1 μsec	Adequate
OFF isolation	60 dB	Low crosstalk
Power supply requirement	±13– ±25 V	High regulation not necessary

ease of operation, the ADC is run at a 100 ms conversion cycle. This signal is derived out of the *Siderial* clock itself for effecting synchronisation with the celestial sources. As seen from Table **3.3,** the time constant of the PSD output is 1 s, *i.e.* the output does not show any si ficant change in amplitude over a period of about 1 s. Hence, as the ADC takes about one-tenth of this time period for its A/D conversion, the amplitude of the signal at its input would essentially remain unchanged.

3.2.3 Programmable-Gain Amplifier (PGA) : As seen earlier, an amplifier with variable gain is required between the MUX and the ADC to exploit the resolution capability of the ADC. Apart from this function, this amplifier has also to serve as a *buffer* to offset the problem of the MUX ON resistance. Since the signal to be *amplified* is the PSD output *i.e. DC,* the variations in gain and offsets of the amplifier are critical in this application. Op-Amp IC type PGA 102 (Burr Brown USA) is a *useful* circuit block here. It has voltage gain values of 1, 10, 100 which are digitally selectable with the logic section functioning from the same supply as that of the amplifier. The range of gain variation achievable here is adequate to take care of the dynamic range of the input signal (Table 3.3). The use of precision laser trimmed offset and gain of this amplifierpermits its use without any external components. The use of thin-film resistors with high temperature tracking in this *IC* assures very low gain drift and good stability, which are necessary in this application. *Important* electrical characteristics of this amplifier are summarised in Table **3.7.** Its pinout is given in Appendix B.

3.2.4 ADC : ADC usually forms the heart of any DAS. There are many techniques for the A/D conversion now a days, and several types of *ADCs* are available in *IC* form to facilitate their use in data acquisition. Desirable characteristics of the *ADC* for use in the data acquisition for this project are:

a) Per channel sampling rate much greater than 1/20 Hz;
   eg.,*10 samples/channel/sec*

b) Good *hum/noise* rejection

c) Resolution better than 1 in 10^3, *i.e.*, 10 bit

TABLE 3.7

PGA - SPECIFICATIONS

parameter	Value (typical)	Remarks
Input impedance	$7 \times 10^8\ \Omega$	Offsets MUX ON resistance
Input voltage swing	± 10 V	No special protection required
Bandwidth	0 - 160 KHz	Well suited
Voltage gain	1, 10, 100	Digitally programmable
CMRR	> 80 dB	Well suited
Settling time	< 2.8 μsec	Fast device
Power supply requirement	f5– f18 V	High regulation not necessary

d) **Low cost and easy availability**

It is evident *from* **Table 2.10 that the ADC most suited for this application is the** *dual* **slope integrating type because of the following benefits:**

a) **Hum rejection by choosing the first integration time period as an** *integral multiple* **of the line period**

b) 12 bit resolution with good accuracy

c) Capability to acquire more than ten samples per second

d) Easy availability and low cost.

Some of the important electrical characteristics of the ADC type *ICL* 7109 *(Intersil* USA) suitable for this application are *summarised* in Table 3.8. Its pinout details are provided in Appendix B. This ADC has 12 bit resolution with separate polarity *and overrange* indication and is microprpcessor compatible. This feature of providing *overrange* information can be effectively used in the dynamic programming of the gain of the PGA to fully exploit the resolution of the ADC. Although the on chip oscillator operates at a frequency which is best suited for rejection of 60 Hz AC, this is isolated here and an external clock has to be supplied to reject 50 Hz, as required in Indian conditions. As the PC bus is byte wise organised, the *parallel* data output of the ADC is preferred for interfacing it with the data storage device. This output is TTL compatible and is available in latched form in the chip itself.

3.2.5 Storage : The memory requirement *(M*, in bytes) for any multi-channel DAS, where no on-line integration or time averaging of the digital data is carried out is generally governed by the following equation:

$$M = N \times (n/8)^{\dagger} \times S \times T \qquad (3.1)$$

Where,

N = number of input channels

n = ADC resolution in bits

TABLE 3.8

ADC - SPECIFICATIONS

Parameter	Value (typical)	Remarks
Input impedance	10 KR	Very low; Buffer necessary
Input voltage swing	± 5, ± 10 V	Decided by R_in
Conversions per sec	30	Only 20 required
Nonlinearity	± 0.2 counts	Adequate
Accuracy	±1/2 LSB	Adequate
CMRR	50μV/V	Good under noisy conditions

S = sampling rate in *samples/sec*

T = total acquisition time in *sec*

† fraction rounded off to higher integer, for realistic conversion to bytes

In this particular application, as $N = 2$, n = 12, S = 10, and $T = 23$ x 40, the required value of M works out to be 36800. As certain additional service bytes (header information like time, date, source name etc.) have also to be stored along with this data, it is estimated that data storage capacity of about 40 Kbytes is adequate per radio source.

As there are about *20* - 25 radio sources, spread over the day, that *can* be observed by this radio interferometer, it is necessary to store the *total* data collected from *all* these sources. This requires a secondary storage device. However, since the access times of most of the secondary storage devices are of the order of *30* - *60* msec, it is preferrable to store the data in a temporary memory until the radio source completes its transit. After this, the entire *40* Kbytes of data can be transfered to a secondary storage device in one operation. It is therefore necessary to provide a suitable RAM in the DAS itself to fulfil this requirement. In this particular application, as the PC was chosen for both to carry out the data acquisition and storage, the RAM of the PC itself could be used for the purpose of temporary data storage. Table **3.9** illustrates the possible memory allocation in a PC having *640* Kbytes of RAM. As the memory requirement for temporary storage is only *a small* fraction of the free RAM usually available in the PC as shown in this Table, it can be accomodated with ease in the *RAM* area of the PC itself This approach not only saves the use of extra memory in the DAS, but also renders it easy for further data handling by the PC using ***DOS*** utilities.

3.2.6 Software : Conventional *DASs* which are built mostly employing *hardware* generally use verylittle *or no* software *(S/W)* at all. On the other hand, DAS based on a PC is associated with software to run the system. In doing so, it is possible to *fully* exploit *all* the features of the various hardware employed in the DAS, and yet have the flexibility to choose to do so. Though it is generally preferred to write the software in a suitable High level language,

TABLE 3.9

POSSIBLE MEMORY ALLOCATION IN PCs

Function / Utility	Allocation in Kbytes (typical)	Remarks
BIOS	20	Always used
DOS shell	65	Always used
User programme	10	Assuming data acquisition S/W
Unused	540	Free memory

in some time critical applications it becomes necessary to develop and use the S/W based on the Assembly **(ASM)** language of the *CPU* employed in the computer. In this application most of the S/W can be developed using the ASM of the *CPU* in the *PCs.*

3.3 Design

A detailed circuit diagram of the DAS evolved as a result of the discussions in the previous section is shown in Fig. 3.4. The important *ICs,* both linear and digital chosen in the design of the **DAS** are listed with their functions as follows:

a) *IH5116 - 16:1* channel analog ***MUX***

b) PG 102 - Programmable gain Op-Amp

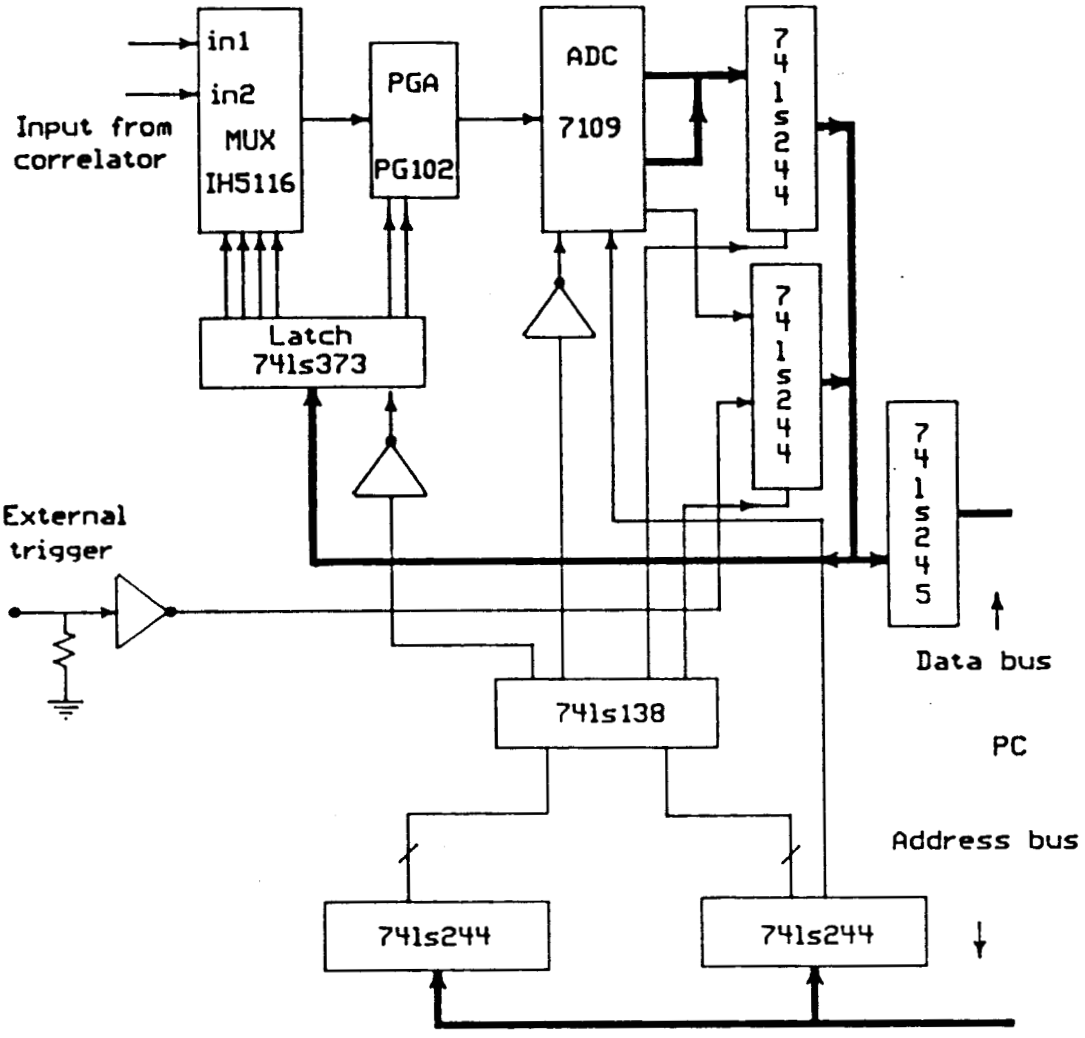


Figure 3.4 Data Acquisition System - Detailed Block Schematic

c) *ICL* 7109 - 12 bit microprocessor compatible, dual-slope ADC

d) *74LS244* - Octal buffer

e) *74LS138* - 3 - 8 line decoder

f) *74LS373* - 8 bit latch

g) TTL Gates

The DAS design is split up into three major hardware functional units based on the nature of the signal handled, and a software module *viz.*

a) *Front* end signal processing

b) A/D conversion with its associated bus interface

c) Timing and control logic

d) Software module

The design of these units is now discussed in detail.

3.3.1 Input Signal Processing : As seen from the previous Sections and Tables 3.4, 3.5 almost all the features required in the MUX and the PGA are fulfilled by standard *ICs.* Normally, the input circuit of a DAS requires protection against unwanted surges etc. However, the *MUX IC* chosen has a built-in input protect mechanism that *automatically* switches off the multiplexing action whenever the input voltage exceeds the supply rail by 10 volts. Therefore no special external protection circuit is required here. The control signals both to the MUX (4 bit) and the PGA (2 bit) have to be supplied by the host PC to exercise full S/W control in the channel and gain selection. Since these control *signals* are directly TTL compatible, no special interfacing circuit is required here. Hence the PC bus is interfaced with ease using a TTL latch configured as an output port to the PC I/O

map, as shown in Fig. 3.5. Here, an 8 bit latch, mapped to one location in the usable I/O space of the P C is made use *of.* For ease of operation, the higher nibble of the data bus is chosen for MUX channel select and the the lower two bits of the lower nibble for PGA gain selection. The logic enable (LE) input of the MUX is not useful in this application as the multiplexing density does not *warrant* the use of more than one IC. However, provision is made for its effective use to syncbronise the sampling operation, as a pulse train external to the P C is chosen for sampling. A *pull-down* resistor (R_1) is required at the sampling input to make the system operational only in the presence of this external *sampling* pulse as shown in the Fig. 3.5. A 470 Ω resistor is adequate for this. The PGA is a self-contained IC with *all* the required facilities built in. Here, no additional interfaces and circuit components *are* required, except for decoupling capacitors. Having multi-*plexed and* suitably amplified the input signal, it is now *available* for A/D conversion.

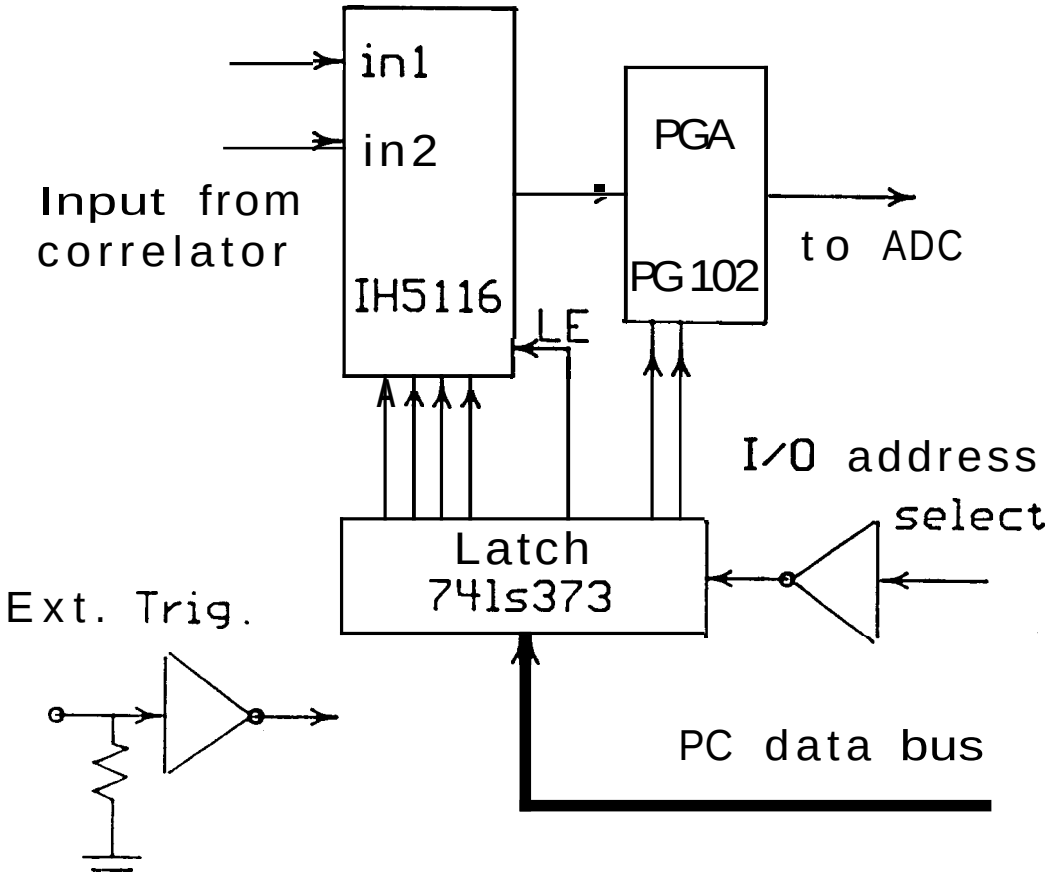
3.3.2 A/D conversion and Bus interface : *The* detailed circuit interconnections of this unit are shown in Fig. ***3.6.*** The signal made available from the front end processing units is directly fed to the ADC for conversion as *shown.* For purposes of flexibility, the ADC IC chosen. $(ICL$ 7109) needs a few external components to configure it for a specific use. These include:

a) *Integra*ting Resistor (R_{int})

b) Integrating Capacitor (C_{int})

c) Auto-Zero Capacitor (C_{az})

d) Reference Capacitor (C_{ref})



Fiqure 3.5 DAS – Input Signal Processing

e) Reference Voltage source (V_{ref})

For optimum performance of the analog section, care must be taken in the selection of these external components both in the choice of their values and their type. The values required in this *particular* application are now calcuated.

Integrating Resistor: The integrator stage of this **ADC** can supply **a** drive current of **20** μ **A** with negligeable non-linearity. The integrating resistor should be large enough to keep within this linear region over the full input voltage range. R_{int} should be chosen by the relation,

$$R_{int} = \frac{full\ \ scale\ \ voltage}{20\ \mu A} \tag{3.2}$$

In this case, for a full scale voltage of $\pm$ 5 V, it works out to be **250** $K\Omega$

Integrating Capacitor: The integrating capacitor C_{int} should be selected to give the maximum integrator output voltage swing (approximately **0.3** volt from either supply) without saturating the integrator. For the **ADC** chosen, operating on $\pm$ 5 V supplies and *analog* ground connected to system ground, a $\pm$ **3.5** to $\pm$ **4** Vintegrator swing is nominal. The clock period chosen has *also* an influence on this capacitor, as the integrating period *takes* **2048** clock pulses. Therefore the value of C_{int} is given by the relation,

$$C_{int} = \frac{(2048\ \text{x}\ \ clock\ \ period)\ (20\ \mu A)}{integrator\ \ output\ \ voltage\ \ swing} \tag{3.3}$$

For a clock of **204.8** ***KHz*** suitable here, the value of C_{int} works out to be $0.05\mu F$. **A 0.047** μF capacitor is used because it is the *nearset* standard value.

An additional requirement of the integrating capacitor is that it should have low dielectric absorption to prevent roll-over errors. Though Teflon capacitors are most suited for this application, Polypropylene capacitors are adequate for temperature ranges below 85° and they axe also reasonably lower in cost. Hence, such a capacitor is chosen for C_{int}.

Auto-Zero Capacitor: The value of the auto-zero capacitor C_{az} has some influence on the noise of the system; *i.e.* the larger the value, the lower the system noise. However, C_{az} cannot be increased without limits since being in parallel with C_{int}, it contributes to the overall R-C time constant that determines the speed of recovery from overloads. Hence for optimal operation, in cases where the input voltage swing is low (eqn. *3.2)*, a value of C_{az} which is twice C_{int} is suitable; and in cases where the input voltage swing is high, C_{az} equal to one half of C_{int} is recomended. In this application as the input voltage range is high, C_{az} value of 0.025 μF is required. Again, from the point of ready availability, C_{az} of 0.027 μF is used here.

Reference Capacitor: A 1 μF capacitor with low leakage characteristics is suggested by the manufacturer for C_{ref} in most applications. However, when a large reference common mode voltage exists *(i.e.* the reference low is not the same as analog ground), and a low input range is chosen, a *larger* value is required to prevent roll-over errors. Hence, C_{ref} of I μF is chosen here.

Reference Voltage source: The analog voltage required to generate a full scale output of 4096 counts (12 bit resolution) is given by,

$$V_{in} = 2 \times V_{REF} \tag{3.4}$$

Hence for a requirement of maximum output counts for an input voltage maximum of 5 V, V_{REF} works out to be 2.5 V. The stability of this reference voltage is a major factor in the overall absolute accuracy of the ADC. The resolution of a 12 bit ADC is one part in 4096, or 224 ppm. Thus if the reference voltage generator has a temperature coefficient of *100ppm/°C*, a temperature difference of *2.5°* C will introduce a one-bit absolute error. Hence depending on the application and the need, a suitable reference voltage generator has to used. In this application a variable *refrenence* generator type MC 1404 (Motorola USA) is adequate.

As seen from the Fig. 3.6, the output of the ADC is *configured* to yield digital data *organised* in byte form. For direct access of this data by the PC, the data bus of the PC has to be suitably interfaced to the ADC output. This requires an *octal* buffer with output tri-state control, as the data output of the ADC is available in latched form. The TTL *IC 74LS244* serves this purpose with IOR (*input/output* read) of the PC qualifying its output tri-state control.

3.3.3 Timing and Control Logic : The sampling pulse being the master clock for all operations in this system, provision has to be made to either use it as an interrupt signal to the PC, or to allow the PC to poll for it and then start its acquisition operation. *In* either case, the sampling pulse triggers off the *mul*tiplexing and A/D conversion processes by the S/W resident in the PC. *In* order to achieve this, the PC bus has to be interfaced to the MUX, the PGA and the ADC with suitable *ICs*. This is shown in the Fig. 3.7. The 8 data and 16 address lines of the PC bus are generally *buffered* before

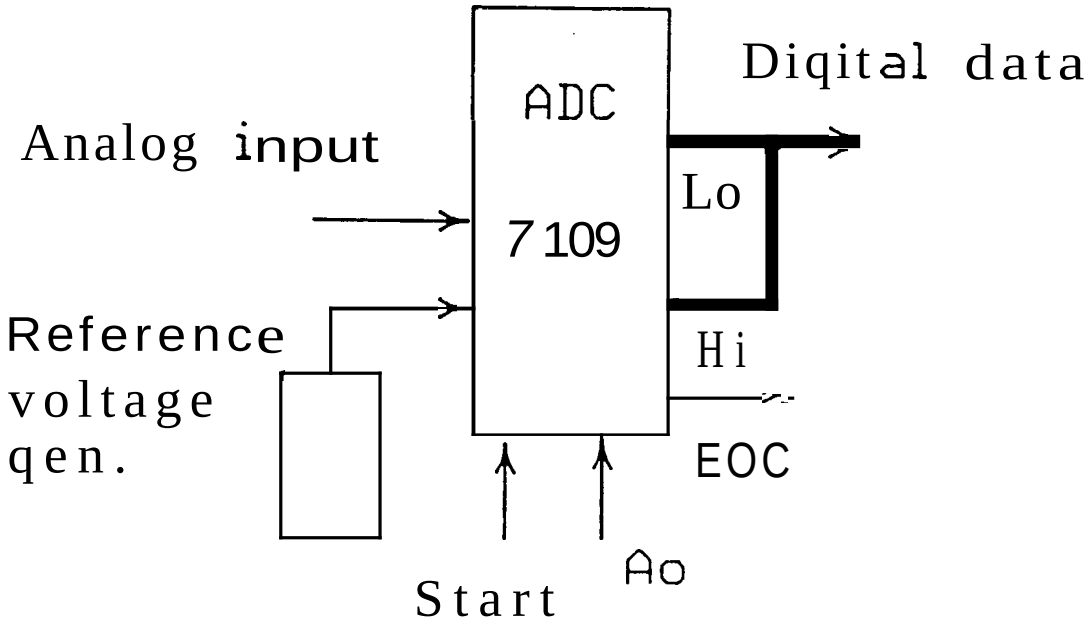


Figure 3.6 ADC - Block Schematic

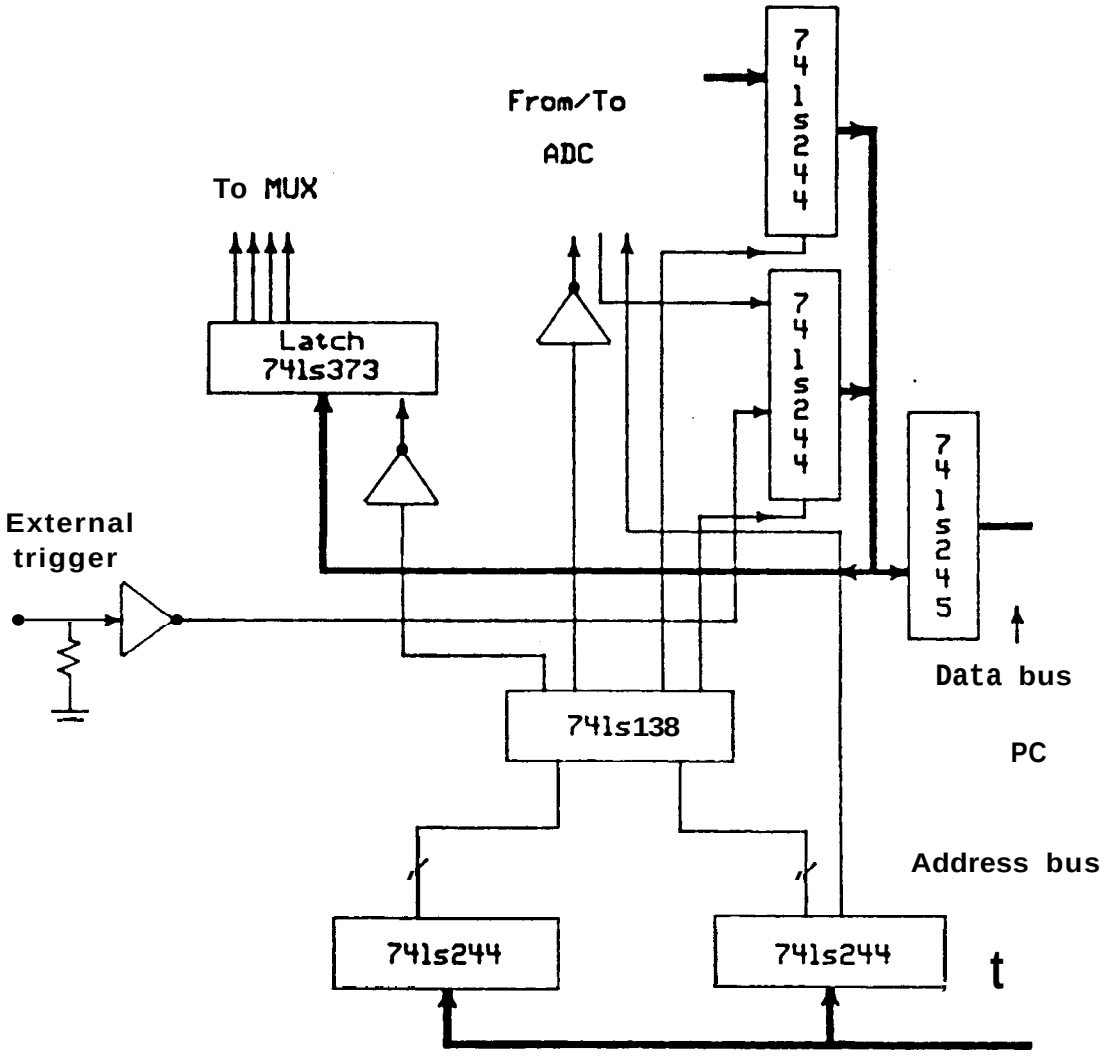


Figure 3.7 DAS - Timing & Control Logic

they are connected to any circuitry for use. This is carried out here with the help of octal buffers (74LS244) as shown. The address lines are decoded to place the octal latch (74LS373) and the ADC in the usable I/O space of the PC using decoder IC (74LS138) and suitable gates.

As all the ICs used in this DAS need a dc supply, a provision has therefore to be made for it. This can be made available either from a separate supply or from the PC bus itself, provided the drain on its logic supply by these ICs is low. As it is convenient to tap off the dc from the PC bus itself, it is necessary to keep the load as low as possible. Hence, TTL ICs of the low power Schotky (74 LS xxx) type have to be used in the implementation of the DAS. Adequate decoupling capacitors (0.1 μF) have to be provided for all the ICs to minirnise the effect of switching transients.

3.3.4 Software Module : The flowchart of the sequence of operations carried out by the software, resident in the PC is given in Figs. 3.8 and 3.9. As is seen from this figure, the software is made up of two parts, *viz.*

a) The main sequence

b) The Interrupt Service Routine (ISR)

The Main Sequence: This section of the software is designed to function interactively with the user/observer, in obtaining information for an observational schedule. Based on the inputs like sampling interval, duration of observation etc., fed in by the user, an unused memory block is allocated for storing the acquired data. The beginning of this block has the header information such as the source name, time, date etc. Upon completing all these functions, the external trigger (sampling pulse) interrupt is enabled

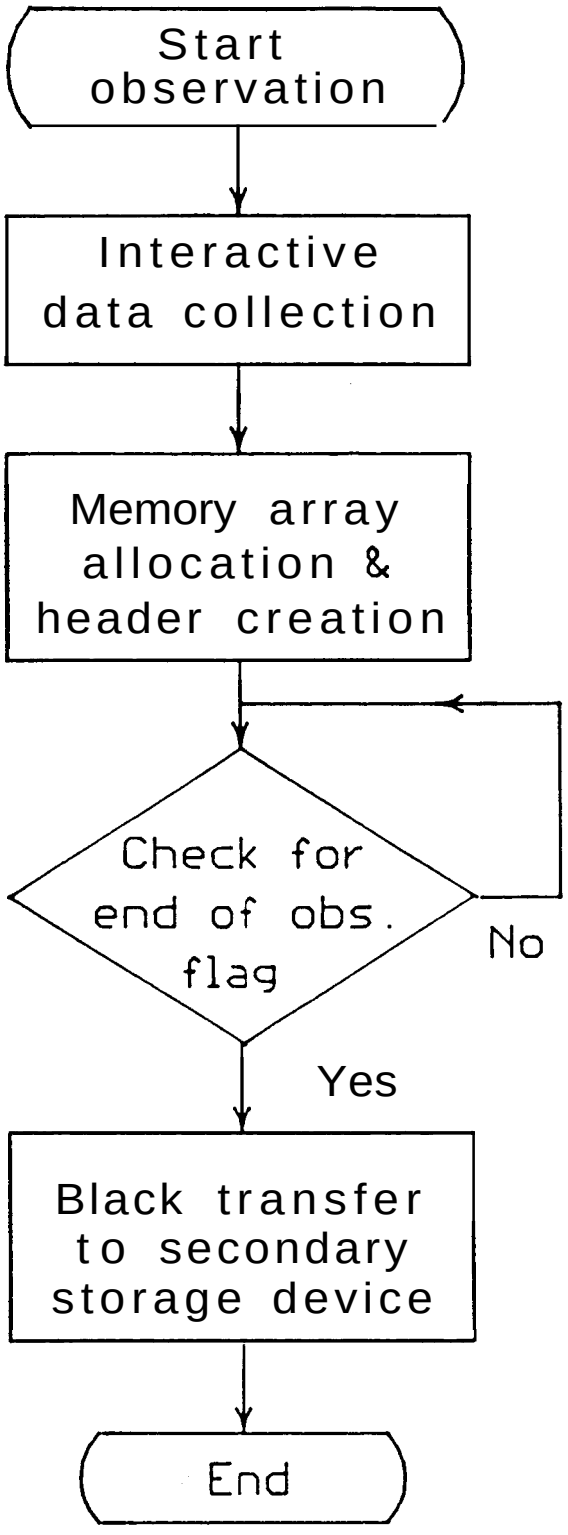


Figure 3.8 Main sequence - Flou-chart

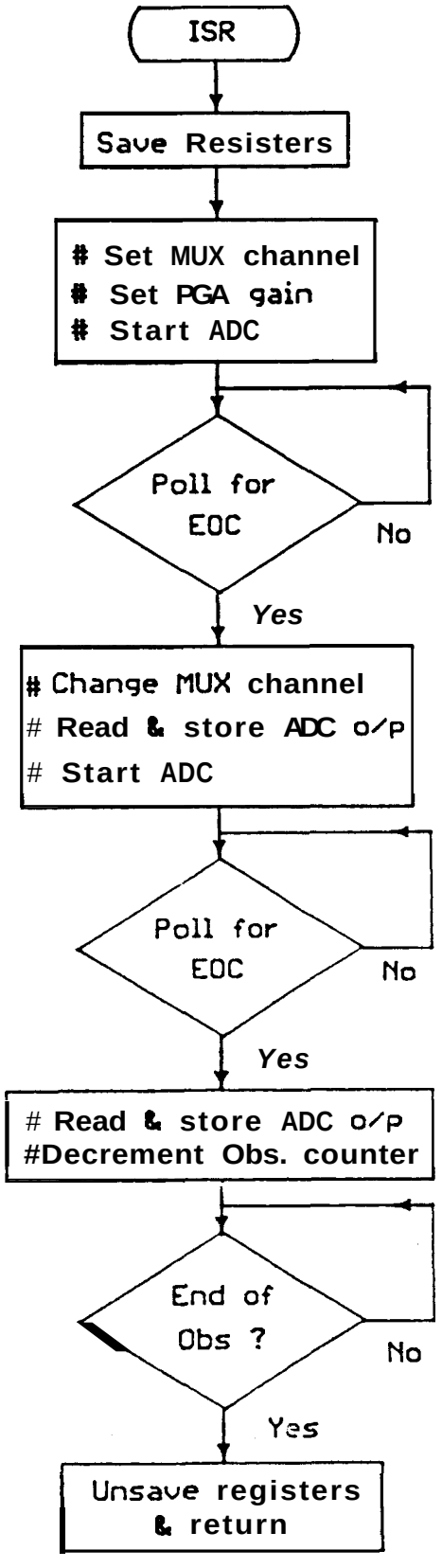


Figure 3.9 Interrupt Service Routine - Flow-chart

and the PC waits to be interrupted.

ISR: This is the real time software and is written in the Assembly language of the microprocessor used in the PCs. This section is invoked by the sampling pulse. In the ISR, the main function is to select the required channel in the MUX, issue a start of convert command to the ADC and wait till the conversion is completed. Then the digital code corresponding to the input signal is read and stored in an appropriate location in the predetermined memory array. This sequence is carried out for both the channels. At the end of this operation, checks are carried out to confirm the end of observation. If the end has not yet been reached, control returns to the main sequence and the system waits for another sampling pulse. If on the other hand an end was detected, the information is flagged before returning to the main sequence. In the main sequence block transfer to secondary storage is initiated, and the acquisition programme comes to a halt by passing the command to DOS residing in the PC.

The design of the hardware and the software of the DAS as explained above is made use of in the experimental work on the interferometer being described in the following chapter.